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# (12) United States Patent Cheng et al.

# (54) HIGH DENSITY VERTICAL NANOWIRE STACK FOR FIELD EFFECT TRANSISTOR

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See application file for complete search history.

### (56) References Cited

#### U.S. PATENT DOCUMENTS

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#### (57) ABSTRACT

An alternating stack of layers of a first epitaxial semiconductor material and a second epitaxial semiconductor material is formed on a substrate. A fin stack is formed by patterning the alternating stack into a shape of a fin having a parallel pair of vertical sidewalls. After formation of a disposable gate structure and an optional gate spacer, raised active regions can be formed on end portions of the fin stack. A planarization dielectric layer is formed, and the disposable gate structure is subsequently removed to form a gate cavity. A crystallographic etch is performed on the first epitaxial semiconductor material to form vertically separated pairs of an upright triangular semiconductor nanowire and an inverted triangular semiconductor nanowire. Portions of the epitaxial disposable material are subsequently removed. After an optional anneal, the gate cavity is filled with a gate dielectric and a gate electrode to form a field effect transistor.

## 9 Claims, 12 Drawing Sheets



